BINDER, SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME, CIRCUIT BOARD, AND ELECTRONIC EQUIPMENT

Technical Field

The present invention relates to a binder, a semiconductor device as well as a method of manufacturing the same, a circuit board, and electronic equipment.

Background of Art

A semiconductor chip and a substrate often differ much in the coefficients of thermal expansion, and particularly when they are cooled after heating, a stress incurred by the difference of the coefficients of thermal expansion is exerted on a binder. Herein, there has been the possibility that the separation of the binder will arise.

Further, in case of employing an anisotropic conductive binder as the binder by way of example, it has sometimes been difficult that an insulating resin is caused to flow out with conductive particles left behind between the bump of the semiconductor chip and a interconnecting pattern formed in the substrate, when the anisotropic conductive film is pressed by the semiconductor chip and the substrate.

These problems are ascribable to the fact that different properties are required for both the surfaces of the binder, and binders in the related art have failed to cope with the requirement.

The present invention consists in solving the problems as

stated above, and has for its object to provide a binder which can cope with the requirement of the different properties for both the surfaces thereof, and a semiconductor device as well as a manufacturing method therefor, a circuit board, and electronic equipment which use the binder.

Disclosure of Invention

(1) A binder according to the present invention is used for bonding electronic components, a physical property of the binder is different in a thickness direction thereof.

Since the physical property differs on both the surfaces of the binder, the binder can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(2) The binder may be an anisotropic conductive film.

Even the anisotropic conductive film can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(3) The binder may form a two-layer structure comprising a first layer formed of a first resin as a base material and a second layer formed of a second resin as a base material, and the first resin and the second resin may have different physical properties.

According to this, the first resin constituting the first layer, and the second resin constituting the second layer have the different physical properties. Thus, the first resin and the second resin can be selected so as to have physical properties respectively suited to a member which adheres to the

first layer, and a member which adheres to the second layer.

(4) In this binder,

a coefficient of thermal expansion of the first resin may be smaller than a coefficient of thermal expansion of the second resin.

When the first layer adheres to the member having the small coefficient of thermal expansion, and the second layer adheres to the member having the large coefficient of thermal expansion, the first and second resins have the coefficients of thermal expansion corresponding to the respective members, and hence, separation hardly occurs.

(5) In this binder,

the silica-based filler may be mixed only in the first resin.

Thus, the coefficient of thermal expansion of the first resin can be made small, and more specifically, it can be brought close to the coefficient of thermal expansion of silicon.

(6) In this binder,

the silica-based filler may be mixed in the first resin and the second resin, and a mixing ratio of the silica-based filler in the first resin may be greater than a mixing ratio of the silica-based filler in the second resin.

Thus, the coefficient of thermal expansion of the first resin can be made smaller than the coefficient of thermal expansion of the second resin, and more specifically, it can be brought close to the coefficient of thermal expansion of silicon.

(7) In this binder,

the second resin may be made lower in elasticity than the first resin.

Thus, when the second layer adheres to the member having the large coefficient of thermal expansion, the second resin is easy of elongation and has a high flexibility, and hence, separation hardly occurs.

(8) In this binder,

the second resin may be a metamorphic epoxy resin.

Thus, the second resin can be made low in elasticity.

(9) In this binder,

the first resin may be an epoxy resin, and

the second resin may be a biphenyl resin.

Thus, the second resin becomes lower in elasticity than the first resin.

(10) In this binder,

conductive particles may be dispersed only in the second resin.

Thus, the conductive particles do not touch the surface of the member adhering to the first layer, and hence, electrical short-circuiting does not occur.

(11) In this binder,

the conductive particles may be dispersed only in the second resin; and

the second layer may be thinner than the first layer, and the second resin may have higher viscosity than the first resin when melted.

According to this, since the conductive particles are dispersed only in the second resin, they do not touch the surface of the member adhering to the first layer, and hence, electrical short-circuiting does not occur. In addition, since the second layer is thinner than the first layer, the electrical short-circuiting can be prevented with the number of the conductive particles decreased. Further, although that the conductive particles are small in number, they can be reliably left behind because of the high melt viscosity of the second resin. Meantime, the first resin lower in the melt viscosity than the second resin is easy to outflow.

(12) In this binder,

the silica-based filler may be mixed only in the second resin.

Thus, the melt viscosity of the second resin can be made higher.

(13) In this binder,

the silica-based filler may be mixed in the first resin and the second resin, and a mixing ratio of the silica-based filler in the first resin may be greater than a mixing ratio of the silica-based filler in the second resin.

Thus, the melt viscosity of the second resin can be made higher.

(14) In this binder,

a molecular weight of the second resin may be greater than a molecular weight of the first resin.

Thus, the melt viscosity of the second resin can be made

higher.

(15) A semiconductor device according to the present invention comprises:

a semiconductor chip;

a substrate on which a interconnecting pattern is formed; and

a binder electrically connecting the semiconductor chip and the interconnecting pattern,

wherein a physical property of the binder being different in a thickness direction thereof.

Since the physical property differs on both the surfaces of the binder, the binder can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(16) In this semiconductor device,

the binder may be an anisotropic conductive film.

Even the anisotropic conductive film can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(17) In this semiconductor device,

the binder may form a two-layer structure comprising a first layer formed of a first resin as a base material and disposed on a side of the semiconductor chip, and a second layer formed of a second resin as a base material and disposed on a side of the substrate, and the first resin and the second resin may have different physical properties.

According to this, the first resin constituting the first layer of the binder, and the second resin constituting the

second layer have the different physical properties. Accordingly, the first resin and the second resin can be selected so as to have physical properties respectively suited to the semiconductor chip which adheres to the first layer, and the substrate which adheres to the second layer.

(18) In this semiconductor device,

the binder may be the binder as mentioned above.

(19) On a circuit board according to the present invention, the semiconductor device as mentioned above is mounted.

(20) Electronic equipment according to the present invention comprises the semiconductor device as mentioned above.

(21) A method of manufacturing a semiconductor device according to the present invention comprises a step of providing a binder between a semiconductor chip and a interconnecting pattern of a substrate on which is formed the interconnecting pattern, pressing the semiconductor chip and the substrate, and electrically connecting the semiconductor chip and the interconnecting pattern,

wherein the binder differs in a physical property in a thickness direction thereof.

Since the physical property differs on both the surfaces of the binder, the binder can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(22) In this method of manufacturing a semiconductor device,

the binder may be an anisotropic conductive film.

Even the anisotropic conductive film can be constructed so as to be suited to materials which are to be bonded to the respective surfaces.

(23) In this method of manufacturing a semiconductor device,

the binder may form a two-layer structure comprising a first layer formed of a first resin as a base material, and a second layer formed of a second resin as a base material, and the first resin and the second resin may have different physical properties.

According to this, the first resin constituting the first layer of the binder, and the second resin constituting the second layer have the different physical properties. Accordingly, the first resin and the second resin can be selected so as to have physical properties suited for adhesion for the semiconductor chip and the substrate.

(24) In this method of manufacturing a semiconductor device,

the second layer may be formed after the first layer.

(25) In this method of manufacturing a semiconductor device,

the first layer may be disposed on a side of the semiconductor chip, and the second layer may be disposed on a side of the substrate.

According to this, the first resin and the second resin can be selected so as to have physical properties respectively suited to the semiconductor chip which adheres to the first

layer, and the substrate which adheres to the second layer.

(26) In this method of manufacturing a semiconductor device,

the binder may be the binder mentioned above.

Brief Description of Drawings

Fig. 1A to Fig. 1C are views showing a method of manufacturing a semiconductor device according to an embodiment of the present invention.

Fig. 2 is a view showing a circuit board according to an embodiment of the present invention.

Fig. 3 is a view showing electronic equipment which includes the semiconductor device manufactured by applying the method according to the present invention.

Best Modes for Carrying Out the Invention

Now, preferred embodiments of the present invention will be described with reference to the drawings.

Fig. 1A to Fig. 1C are views showing a method of manufacturing a semiconductor device according to an embodiment the present invention. Shown in Fig. 1C is the semiconductor device 1 finished up by the manufacturing method.

The semiconductor device 1 includes a semiconductor chip 10 and a substrate 20. In a case where the planar shape of the semiconductor chip 10 is a rectangle (a regular square or an oblong), a plurality of electrodes 12 are formed on one surface (active surface) of the semiconductor chip 10 along "at least

one edge" (comprehending "two opposing edges" or "all edges"). Alternatively, a plurality of electrodes 12 may well be formed on the central part of one surface of the semiconductor chip 10. The electrodes 12 are often provided with bumps 14 by solder balls, gold wire balls, gold plating or the like, but this is not indispensable. The electrodes 12 themselves may well be in the shape of bumps. Nickel, chromium, titanium or the like may well be added between the electrodes 12 and the bumps 14 as a layer preventive of the diffusion of a bump metal.

The shape of the whole substrate 20 may be any of a rectangle, a polygon, or a shape with a plurality of rectangles combined, without being especially restricted, and it can be made similar to the planar shape of the semiconductor chip 10. Although the thickness of the substrate 20 is often determined by the quality of the material thereof, it is not restricted, either. The substrate 20 may be formed of any of organic type and inorganic type materials and may well be made of a composite structure of these materials, but preferably it can be punched through. The substrate 20 can be formed by punching through a tape-like flexible substrate which is formed of an organic type material.

A multilayer substrate or a build-up type substrate may well be employed as the substrate 20. In case of utilizing the build-up type substrate or the multilayer substrate, when a interconnecting pattern is formed on a ground layer spreading planarly, a microstrip structure having no surplus interconnecting pattern is obtained, and hence, the transmission characteristics of signals can be enhanced.

A plurality of interconnections (leads) are formed on one surface of the substrate 20, thereby to construct the interconnecting pattern 22. At least one or all of the plurality of interconnections is/are not in electrical conduction with any other interconnection, and is/are electrically independent. Alternatively, those of a plurality of interconnections which are connected to the common locations, such as power supply and ground, of the semiconductor chip 10 may well be interconnected. Land portions are formed at both the ends of each interconnection. Each of the land portions is often formed so as to have a width greater than that of the portion which connects between both the land portions. It is also allowed to form one of the land portions at that position of the substrate 20 which is near the end part of the semiconductor device being the final product, and to form the other land portion at that position of the substrate 20 which is near the central part thereof. Bumps may well be formed at those parts (for example, the land portions) of the interconnecting pattern 22 which are bonded with the electrodes 12 of the semiconductor chip 10. In that case, the bumps 14 of the semiconductor chip 10 can also be omitted.

A plurality of through holes 24 are formed in the substrate 20. The interconnecting pattern 22 is so formed that any of the interconnections passes on each of the through holes 24. The end part of the interconnection may well overlie the through hole 24. In a case where the land portion is formed at the end part of the interconnection, it overlies the through hole 24.

As shown in Fig. 1C, the substrate 20 is provided with external terminals 40. Solder balls may well be used as the external terminals 40. The external terminals 40 are electrically connected to the interconnecting pattern 22. The external terminals 40 can be electrically connected to the interconnecting pattern 22 by, for example, providing conductive members in the through holes 24 by plating or the like, or disposing a solder in the through holes.

Plating is performed for the interconnecting pattern 22. The interconnecting pattern 22 can be formed of copper, and plated with nickel, gold, a solder or tin. A conductivity is ensured by performing the plating. Concretely, good soldering with the external terminal 40 is permitted, the oxidation of the surfaces of the interconnection is prevented, and the resistance of electrical connection with the bump is lowered.

The semiconductor chip 10 is mounted on the substrate 20 in face-down fashion. The bumps 14 of the semiconductor chip 10 and the interconnecting pattern 22 formed on the substrate 20 are electrically connected. In the present invention, the external terminals 40 stated above are not always necessary. Required, at least, is a construction which has the semiconductor chip 10 and the substrate 20 formed with the opposing interconnecting pattern 22, and in which a binder 30 exists between the semiconductor chip 10 and the substrate 20. The binder 30 may be, at least, of a resin (an underfill resin) having an insulating property, and it may well be of a resin having an anisotropic conductivity. Regarding the face-down

bonding between the bumps 14 of the semiconductor chip 10 and the interconnecting pattern 22 of the substrate 20, there have been known a method which is based on intermetallic bonding with a brazing material such as solder, or the like, a method which holds a mechanical bonding strength by utilizing the shrinkage of a resin, a method which heats and presses the semiconductor chip bearing the gold bumps (if necessary, ultrasonic bonding is performed), a method which employs an anisotropic conductive film, and so forth, and any of the methods may be applied.

The binder 30 forms a two-layer structure which comprise a first layer 32 and a second layer 34. The first layer 32 is made of a first resin, while the second layer 34 is made of a second resin. In this embodiment, the first resin and the second resin have different physical properties. Shown in Fig. 1A is an example in which the anisotropic conductive film is used as the binder 30. The binder 30 is such that conductive particles 36 are dispersed in a binder.

(The case where the coefficients of thermal expansion are different)

The coefficient of thermal expansion of the first resin (for example, 20 to 40 (10^{-6}/°C)) may well be smaller than the coefficient of thermal expansion of the second resin (for example, 40 to 200 (10^{-6}/°C)). The first layer 32 made of the first resin adheres to the semiconductor chip 10, while the second layer 34 made of the second resin adheres to the substrate 20. Here, the semiconductor chip 10 is often made of a material

of which coefficient of thermal expansion is small (for example, silicon), while the substrate 20 is often made of a material of which coefficient of thermal expansion is large (for example, a polyimide resin).

The difference of the coefficients of thermal expansion is small between the first layer 32 made of the first resin having the small coefficient of thermal expansion and the semiconductor chip 10 having the small coefficient of thermal expansion, so that the separation of the binder 30 is difficult to occur. In order to bring the coefficient of thermal expansion of the first resin close to the coefficient of thermal expansion of silicon, a silica-based filler may well be mixed in the first resin at a mixing ratio of, for example, 30% to 60%. In that case, the silica-based filler should preferably be prevented from mixing in the second resin. Alternatively, even when the silica-based filler is mixed in the first resin and the second resin, the mixing ratio of the silica-based filler in the first resin may be greater than that of the same in the second resin. In that case, the difference of the mixing ratios of the silica-based filler should preferably be on the order of 30% to 60%.

The difference of the coefficients of thermal expansion is small between the second layer 34 made of the second resin having the large coefficient of thermal expansion and the substrate 20 having the large coefficient of thermal expansion, so that the separation of the binder 30 is difficult to occur.

In the case where the anisotropic conductive film is

employed as the binder 30, and where the coefficients of thermal expansion of the first and second resins are different, the conductive particles 36 may well be dispersed in only one of the resins. Concretely, the conductive particles 36 should preferably be dispersed only in the second layer 34 which adheres to the interconnecting pattern 22 having an electrical connection area larger than that of the bumps 14 of the semiconductor chip 10. Thus, when the bumps 14 have sunk in the binder 30 (anisotropic conductive film), the probability at which the conductive particles 36 remain under the bumps 14 heightens to enhance the reliability of electrical connections. Moreover, since the conductive particles 36 are not dispersed in the first layer 32 adhering to the semiconductor chip 10, the short-circuiting between the electrodes 12 of the semiconductor chip 10 is prevented.

(The case where the elastic moduli are different)

The second resin may well be made lower in elasticity than the first resin. By way of example, it is also allowed that the elastic modulus of the first resin is about 3 to 10 (GPa), while the elastic modulus of the second resin is about 1 GPa to 3 GPa. Thus, when the second layer 34 made of the second resin adheres to the substrate 20 having the large coefficient of thermal expansion, the second resin is easy of elongation and has a high conformability, so that the separation becomes difficult to occur.

In order to lower the elasticity of the second resin, an

epoxy resin may well be metamorphosed as such. Alternatively, it is also allowed that the first resin is the epoxy resin, while the second resin is a biphenyl resin.

Also in the case where the anisotropic conductive film is employed as the binder 30, and where the elastic moduli of the first and second resins is different, the conductive particles 36 may well be dispersed in only one of the resins. Concretely, the conductive particles 36 should preferably be dispersed only in the second resin constituting the second layer 34 which adheres to the interconnecting pattern 22 having an electrical connection area larger than that of the bumps 14 of the semiconductor chip 10. Thus, when the bumps 14 have sunk in the binder 30, the probability at which the conductive particles 36 remain under the bumps 14 heightens to enhance the reliability of electrical connections. Moreover, since the conductive particles 36 are not dispersed in the first resin constituting the first layer 32 adhering to the semiconductor chip 10, the short-circuiting between the electrodes 12 of the semiconductor chip 10 is prevented.

(The case where melt viscosities are different)

In the case of employing the anisotropic conductive film as the binder 30, the second resin may well be higher than the first resin in the viscosity of a melted state. Thus, when the bumps 14 have sunk in the binder 30, the first resin of low melt viscosity is easy of outflow, and the second resin of high melt viscosity is difficult of outflow. Since the melt viscosity

of the second resin is high, the conductive particles 36 are easy to remain on the interconnecting pattern 22. In this case, the conductive particles 36 may well be dispersed in only the second resin constituting the second layer 34 which adheres to the interconnecting pattern 22. Since the conductive particles 36 are not dispersed in the first resin constituting the first layer 32 adhering to the semiconductor chip 10, the short-circuiting between the electrodes 12 of the semiconductor chip 10 is prevented.

Further, the second layer ~~32~~ 34 may well be thinner than the first layer ~~34~~ 32. Thus, the electrical short-circuiting can be prevented with the number of the conductive particles 36 decreased, and notwithstanding that the conductive particles 36 are small in number, they can be reliably left behind on the interconnecting pattern 22 owing to the high melt viscosity of the second resin.

In the case of employing the anisotropic conductive film as the binder 30, a silica-based filler may well be mixed in only the second resin in order to make the melt viscosity of the second resin higher than that of the first resin. Alternatively, it is also allowed to mix the silica-based filler in the first resin and second resin, and to make the mixing ratio of the silica-based filler in the second resin greater than that of the same in the first resin. Alternatively, it is also allowed to set the molecular weight of the second resin larger than that of the first resin.

While, in the above, the two layers of resins having the

different physical properties have been stated as to this embodiment, the difference of the physical properties between the layers should more preferably change continuously, not stepwise, and this is more meritorious because the difference of the physical properties in the thickness direction of the layers is not existent. The reason is that the separation, etc. ascribable to the difference of the physical properties at the interface of the two layers are difficult to arise. Concretely, multilayer resins of which physical properties are different with small differences, or resins of which physical properties change continuously in the thickness direction thereof can be used for that purpose.

Two layers of anisotropic conductive films are obtained in such a way that a single layer of anisotropic conductive film is prepared in the shape of a sheet, whereupon a single layer of anisotropic conductive film having a different physical property is further prepared on the first-mentioned layer in the shape of a sheet. The subsequent handling is the same as in the single layer of anisotropic conductive film. In case of more layers of anisotropic conductive films, these operations are repeated. In forming an anisotropic conductive film of which physical property differs continuously in the thickness direction thereof, the interdiffusion between layers is induced by solvents which are used when the two or more layers of anisotropic conductive films are prepared, or by some heating. Thus, the continuous layer can be obtained.

The semiconductor device according to this embodiment is

constructed as stated above, and a method of manufacturing it will be described below.

As shown in Fig. 1A, the surface of a semiconductor chip 10 formed with electrodes 12 (or bumps 14) and the surface of a substrate 20 formed with a interconnecting pattern 22 are disposed so as to oppose to each other. In addition, a binder 30 is disposed between the semiconductor chip 10 and the substrate 20. More specifically, the binder 30 is interposed with its first layer 32 confronted to the semiconductor chip 10 and its second layer 34 confronted to the substrate 20. Incidentally, the binder 30 should preferably be stuck onto either of the semiconductor chip 10 and the substrate 20 beforehand.

In a case where the binder 30 formed of a plurality of layers (for example, the two layers of first and second layers 32, 34), the respective layers of the plurality of layers (for example, the first layer 32 and the second layer 34) may well be disposed in succession. More specifically, it is also allowed to successively dispose the layers by attaching the corresponding layer to either the semiconductor chip 10 or the substrate 20, or to attach either layer (for example, the first layer 32) to the semiconductor chip 10, followed by attaching the other layer (for example, the second layer 34) to the substrate 20.

As shown in Fig. 1B, the semiconductor chip 10 and the substrate 20 are brought into adhesion through the binder 30. More specifically, the semiconductor chip 10 and the substrate 20 are pressed in the direction of narrowing the spacing between

the two. Thus, conductive particles 36 are interposed between the electrodes 12 (or bumps 14) of the semiconductor chip 10 and the interconnecting pattern 22, whereby the electrical connections between the two are established.

As shown in Fig. 1C, external terminals 40 are provided on the substrate 20, whereby the semiconductor device 1 can be obtained. Although the semiconductor device of FAN-IN type in which the external terminals 40 are disposed only within the mounting area of the semiconductor chip 10 is shown in Fig. 1C, the present invention is not restricted thereto. The present invention is also applicable to, for example, a semiconductor device of FAN-OUT type in which external terminals 40 are disposed only outside the mounting area of the semiconductor chip 10, and a semiconductor device of FAN-IN/OUT type in which the FAN-OUT type is combined with the FAN-IN type. By the way, in the semiconductor device of the FAN-OUT type or the FAN-IN/OUT type, a stiffener may well be stuck outside the semiconductor chip by employing an anisotropic conductive film.

In this embodiment, the binder 30 comprising the first and second layers 32, 34 is used, so that the effects stated above can be accomplished.

Although this embodiment has been described concerning the example in which the semiconductor chip 10 is mounted on the substrate 20 of BGA (Ball Grid Array) type in face-down fashion, it is as stated before that, without regard to the structural aspect of the substrate 20, the invention can be applied to any mounting aspect in which the semiconductor chip 10 is merely

subjected to the face-down mounting on the substrate 20.

Shown in Fig. 2 is a circuit substrate 50 in which the semiconductor device 1 according to this embodiment is mounted. It is common to employ an organic type substrate, for example, a glass epoxy substrate, as the circuit board 50. A interconnecting pattern 52 made of, for example, copper is formed in the circuit board 50 so as to become a desired circuit, and the interconnecting pattern and the external terminals 40 of the semiconductor device 1 are mechanically connected, thereby to attain the electrical conduction thereof.

Besides, a notebook type personal computer is shown in Fig. 3 as electronic equipment 60 having the semiconductor device 1 to which the present invention is applied.

Incidentally, an electronic component can also be manufactured by substituting an "electronic element" for the constituent requisite "semiconductor chip" of the present invention and mounting the electronic element (irrespective of whether it is an active element or a passive element) on a substrate likewise to the semiconductor chip. The electronic component which is manufactured using such an electronic element is, for example, a resistor, a capacitor, a coil, an oscillator, a filter, a temperature sensor, a thermistor, a varistor, a volume controller or a fuse.